70% High Efficient C-Band 27W Hetero-structure FET for Space Application

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Abstract — **A highly reliable and 70% highly efficient C-Band 27W internally-matched GaAs FET with a total gate width of 18.9mm x 4 has been developed for space applications. The newly developed Hetero-structure FET (HFET) successfully reduces the gate leakage current even for RF overdrive region, which is indispensable to improve the power-added efficiency and reliability, simultaneously. The bias conditions and the 2nd harmonic tuning for both the input and output matching circuits are also optimized to increase high efficiency. No failure in reliability tests was observed under RF operation based on the European Space Agency Specification (ESA) and RF overdrive at 5dB compression. These excellent results promise that the newly developed HFET can replace the conventional traveling-wave tube amplifiers (TWTAs) for space applications.**

I. INTRODUCTION

In order to replace the conventional traveling-wave tube amplifiers (TWTAs) by the solid-state power amplifiers (SSPAs), highly reliable and highly efficient GaAs FETs had been aggressively developed. A highly reliable 50% efficiency C-Band 27W internally -matched GaAs FET have already obtained [1]. However, the efficiency of the GaAs FET is inferior to that of the TWTAs, though the size, the weight and the mechanical shook in the GaAs FET is superior to them of the TWTAs. Furthermore the improvement of efficiency with keeping high reliability has been required, in order to promote the replacement. We have successfully developed a highly reliable and 70% efficient C-Band 27W internally matched GaAs HFET with a total gate width 18.9mm x 4.

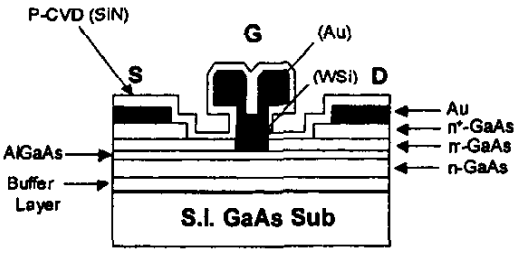
These excellent results are derived from the optimization of 2nd harmonic tuning in both input and output circuits [2],[3] and the bias condition, combined with the reduction of the gate leakage currents.

In this paper, we describe the newly developed HFET structure, the dependence of the efficiency on the 2nd harmonic phase and also the extremely stable reliability test results based on ESA.

II. CHIP STRUCTURE AND DESIGN

In order to obtain high efficiency, it is important to achieve the high gain and breakdown voltage simultaneously. We have already developed the high performance HFET for the base station at L/S-Band [4]. The developed FET structure was optimized at C-Band operation which is based on the HFET.

Figure 1 shows a cross section of newly developed Hetero-structure FET (HFET). The developed FET structure consist of the WSi/Au T-shaped buried gate, AlGaAs Schottky layer and recess structures by using selective etching process. To reduce the thermal resistance, a gold Plated Heat Sink (PHS) structure was adopted on the backside of wafer. The thickness of PHS Au layer and GaAs substrate was 30um and 40um respectively. The gate length and channel carrier concentration was 0.6um and 1.5E17, respectively. The total gate width (Wgt) of HFET chip is 18.9mm which consists of 9cells. Each cell has 14-fingers with 150um length. The chip size is 0.53 x 2.31mm^2.



G : Gate , S : Source , D : Drain

Figure 1 Schematic cross section of HFET

III. CIRCUIT DESIGN

In order to achieve 70% high efficiency C-Band 27W internally-matching GaAs FET, the four 18.9mm FET chips were combined in parallel and the source and load-pull measurement of 1chip was performed by using the 2nd harmonic tuning. We employed the two-stage for input and output matching circuits that consists of multisection quarter-wavelength impedance transformers. On 1st stage transmission line with low impedance, we performed the Source and Load-pull measurement of 1chip and optimized the low impedance by using the 2nd harmonic tuning.

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Figure 2 shows the dependence of peak power-added efficiency on the source phase at the 2nd harmonic frequency. In this way, we experimentally obtained the optimum 2nd harmonic source impedance. The design target impedance was estimated by using source and load-pull measurement of 1chip cell. In addition, gate bias condition was optimized to class-AB operation (Ids=1/7Idss).

Figure 3 shows the internal view of developed C-Band internally-matched GaAs FET. The package size is 24.0 x 17.4 x 4.4 mm^3 and four 18.9mm FET chips are combined in parallel.

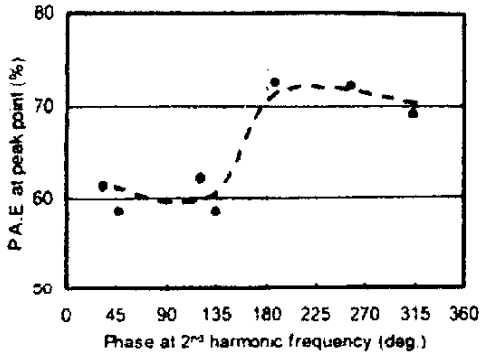

Figure 2 Measured power-added efficiency at peak point versus the source phase at 2nd harmonic frequency

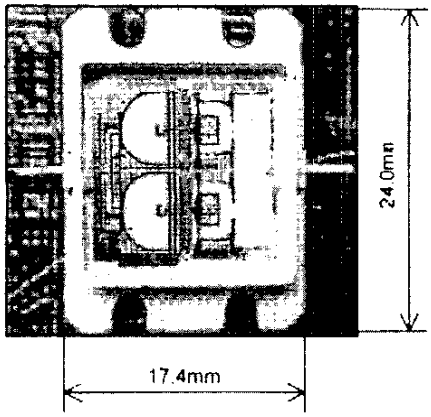

Figure 3 The internal view of developed C-Band internally-matched GaAs FET

IV. RF PERFORMANCE

Figure 4 shows the measured output power and power-added efficiency (PAE) versus input power of C-band FET by using FET chips at 3.85GHz. A saturation power of 44.1dBm (27W) and peak PAE of 70.6% was achieved with linear gain of 14.0dB at 3.85GHz and at drain-source voltage (Vds) of 9.5V, drain-source current (Ids) of 1/7Idss.

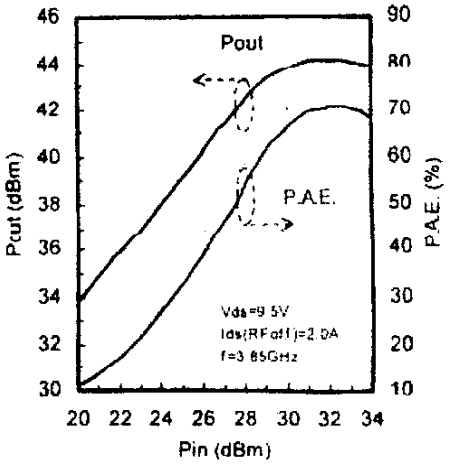

Figure 4 Measured output power and power-added efficiency (PAE) versus input power of C-band FET at 3.85GHz

V. RELIABILITY

For space application, the reliability is the most important consideration. The generally conventional device screening was applied the RF Burn-in. However, the newly device screening has been applied the DC Burn-in added the Room Temperature RF overdrive (RTRF) in the conditions of Vds=14.0V and 10dB-gain compression and we has confirmed the stability of FETs. Table 1 shows the conventional and newly device screening flow of FETs.

Table 1 The device screening flow of FETs

(a) conventional	(b) newly
Assembly	Assembly
	RTRF
DC/RF measurement	DC/RF measurement
HTRB *	HTRB *
DC/RF measurement	DC/RF measurement
RF Burn-in	DC Burn-in
DC/RF measurement	DC/RF measurement
Delta judgment	Delta judgment

* : HTRB (High Temperature Reverse Bias)

The RF operation life test (Tch=175degC) and the environment test for power device was performed according to ESA. In addition of the RF operation life test, the RF overdrive life test was performed in conditions of 5dB gain compression. Table 2 shows the

detail conditions of RF operation life test and RF overdrive life test. The 1dB-gain compression output power (P1dB) was measured at the interim point of 1000, 2000hrs and finally 3000hrs.

Table 2 The conditions of RF life test

test	test conditions
RF operation life test	Tch=175deg.C , Vds=10V , 25%Idss P2dB drive , f=3.95GHz , 3000hrs
RF overdrive life test	Ta=25deg.C , Vds=9V , 25%Idss P5dB drive f=3.95GHz , 3000hrs

Figure 5 and 6 shows 1dB-gain compression output power during the RF life test that we could confirm the stability of FETs during 3000hrs on the RF operation life test and the RF overdrive life test. At present, there has been no failure so that the failure mode and/or MTTF can't be determined.

We conclude that the high reliability of Hetero-structure FET device has been achieved from the results of RF operation life test and RF overdrive life test. By performing the device screening with the RF overdrive and DC power Burn-in the effect of screening is the same as the RF power Burn-in and/or better than it.

VI. CONCLUSIONS

A C-Band 27W internally matched GaAs FET has been developed with the Hetero-structure FET chips for space applications. The FET exhibits a linear gain of 14.0dB, saturation power of 44.1dBm (27W), power-added efficiency of 70.6% at 3.85GHz. We confirmed that C-Band 27W FETs are stable during 3000hrs on the reliability test based on ESA and RF overdrive operation at the condition of 5dB compression.

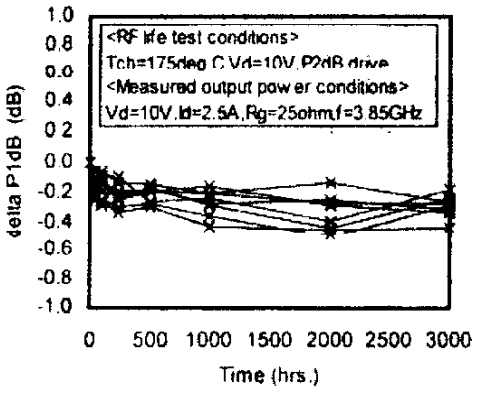

Figure 5 1dB-gain compression output power during the RF operation life test (Tch=175deg.C)

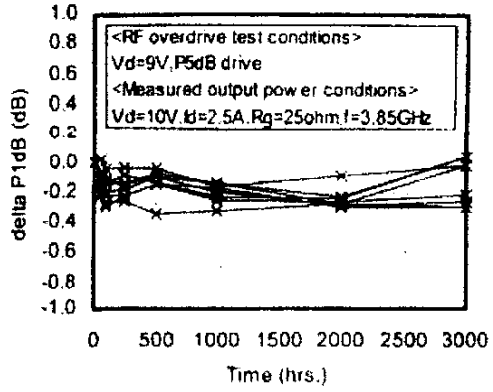

Figure 6 1dB-gain compression output power during the RF overdrive life test

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